AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims

1-14 (Cancelled)

15. (New) A semiconductor integrated circuit comprising:

a first operating unit which has a first nonvolatile memory to which a first program is stored, and a control unit generating a first key code in accordance with the first program;

an encryption unit which has a first register and which encrypts communication data in accordance with the first key code stored in the first register;

an interface unit which communicates in accordance with a predetermined protocol; and

an internal bus which is coupled to the first operating unit, the encryption unit, and the interface unit,

wherein the first nonvolatile memory, the control unit, the encryption unit, the interface unit, and the internal bus coupled to the first nonvolatile memory and the control unit are formed on a single semiconductor chip,

wherein the first operation unit performs a first operation in which the control unit reads out the first program from the first nonvolatile memory, a second operation in which the control unit generates the key code in accordance with the first program, and a third operation in which the control unit sets the first key code to the first register via the internal bus, on the single semiconductor chip.

16. (New) A semiconductor integrated circuit comprising:

a main processing unit which generates a first key code according to a predetermined algorithm, which determines approval/non-approval of an outside device, and which controls communication between the semiconductor integrated circuit and the outside device in a state

of the approval;

an encryption unit which has a first register and which encrypts communication data in accordance with the first key code stored in the first register;

an interface unit which performs the communication with the outside device, in accordance with a predetermined protocol and the approval; and

an internal bus which is coupled to the main processing unit, the encryption unit and the interface unit;

wherein the main processing unit, the encryption unit, the interface unit and the internal bus are formed on a single semiconductor chip,

wherein the main processing unit sets the first key code to the first register via the internal bus.

17. (New) A semiconductor integrated circuit according to claim 16, further comprising:

a first nonvolatile memory to which a first program for generating the first key code and for determining the approval/non-approval of the outside device is stored; and

a volatile memory which is as a work area for the main processing unit,

wherein the internal bus is coupled to the first nonvolatile memory and the volatile memory.

18. (New) A semiconductor integrated circuit according to claim 17, further comprising:

a second nonvolatile memory to which a communication control program and a unique information related to a device is stored,

wherein the interface unit which has a second register to which a second key code for determining the approval/non-approval of the outside device is stored,

wherein the main processing unit generates the second key code in accordance with the first program,

wherein the main processing unit controls the communication between the semiconductor integrated circuit and the outside device in the state of the approval, in accordance with the communication control program, and

wherein the internal bus is coupled to the second nonvolatile memory.

19. (New) A semiconductor integrated circuit according to claim 17, further comprising a bus control circuit which controls the internal bus,

wherein the bus control circuit is between the internal bus and an outside of the semiconductor integrated circuit.

20. (New) An electric device comprising:

a semiconductor integrated circuit which includes;

a main processing unit which generates a first key code according to a predetermined algorithm, which determines approval/non-approval of an outside device, and which controls communication between the semiconductor integrated circuit and the outside device in a state of the approval;

an encryption unit which has a first register and which encrypts communication data in accordance with the first key code stored in the first register;

a first interface unit which performs the communication with the outside device, in accordance with a predetermined protocol and the approval;

a second interface unit;

a communication circuit; and

an internal bus which is coupled to the main processing unit, the encryption unit, the second interface unit, the communication circuit and the first interface unit;

a host unit which controls the electric device and communicates to the communication circuit; and

an external device coupled to the second interface unit,

wherein the main processing unit; the encryption unit, the first interface unit, the second interface unit, the communication circuit and the internal bus are formed on a single semiconductor chip, and

wherein the main processing unit sets the first key code to the first register via the internal bus.

21. (New) The electric device according to claim 20, further comprising:

an external memory,

wherein the semiconductor integrated circuit has a bus control unit coupled to the internal bus, and

wherein the bus control unit coupled to the external memory controls the internal bus.

22. (New) The electric device according to the claim 20, further comprising:

a first nonvolatile memory to which a first program for generating the first key code and for determining the approval/non-approval of the outside device is stored; and

a volatile memory which is as a work area for the main processing unit,

wherein the internal bus is coupled to the first nonvolatile memory and the volatile memory.

23. (New) The electric device according to claim 20, further comprising:

a second nonvolatile memory to which a communication control program and an unique information of the electric device is stored,

wherein the interface unit which has a second register to which a second key code for determining the approval/non-approval of the outside device is stored, and the main processing unit generates the second key code in accordance with the first program, wherein the main processing unit controls the communication between the semiconductor integrated circuit and the outside device in the state of the approval, in accordance with the communication control program, and

wherein the internal bus is coupled to the second nonvolatile memory.

24. (New) The semiconductor integrated circuit according to claim 15,

wherein an encryption unit de-encrypts data in accordance with a key code stored in the first register.

25. (New) The electric device according to claim 20,

further comprising an encryption unit that de-encrypts data in accordance with a key code stored in the first register.